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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/583,501	06/19/2006	Kazuhiro Fujikawa	12967-007US1 905350-02	3685

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EXAMINER	
YUSHINA, GALINA G	
ART UNIT	PAPER NUMBER
2811	

NOTIFICATION DATE	DELIVERY MODE
07/24/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PATDOCTC@fr.com

Office Action Summary	Application No.	Applicant(s)	
	10/583,501	FUJIKAWA ET AL.	
	Examiner	Art Unit	
	GALINA YUSHINA	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 June 2009* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☒ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figures 6 and 7 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. **The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102** that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. **Claims 1-4 and 7-8 are rejected under 35 U.S.C. 102(b)** as being anticipated by Iwasaki et al. (US 2005/0006649).

4. **In re Claim 1**, Iwasaki teaches a junction field-effect transistor (Abstract, Fig. 5) comprising:

- a first conductivity type (n-type, paragraph 0035) semiconductor layer (2, paragraphs 0035, 0038) having a channel region (designated by Wlch and Wvch, paragraph 0035);
- a buffer layer (51, paragraph 0038) formed on said channel region (designated by Wlch and Wvch); and
- a second conductivity type (p-type) doped region (52, paragraph 0038) formed on said buffer layer (51), wherein
- a first conductivity type (n-type) carrier concentration in said buffer layer (51) is lower than a first conductivity type (n-type) carrier concentration in said first conductivity type semiconductor layer (2) (a buffer layer 51 is a p-doped layer, paragraph 038).

5. **In re Claim 2**, Iwasaki teaches that said first conductivity type (n-type) carrier concentration in said buffer layer (51, paragraph 0038) is not more than one tenth of said first conductivity type carrier concentration in said first conductivity type semiconductor layer (2, paragraph 0035) (a buffer layer 51 contains only p-dopants, paragraph 0038).

6. **In re Claim 3**, Iwasaki teaches that said first conductivity type semiconductor layer (2, paragraph 0035) is composed of silicon carbide (paragraphs 0035 and 0037).

7. **In re Claim 4**, Iwasaki teaches the junction field-effect transistor according to Claim 1, further comprising a second conductivity type (p-type) semiconductor layer (3, paragraph 0035) formed under said channel region (designated by Wlch and Wvch, paragraph 0035).

8. **In re Claim 7**, Iwasaki teaches the junction field-effect transistor according to Claim 1, further comprising:

- a semiconductor substrate (1, paragraph 0035) composed of n-type silicon carbide (paragraphs 0035 and 0037), wherein
- said first conductivity type semiconductor layer (2, paragraph 0035) is formed on one main surface (the upper surface) of said semiconductor substrate (1).

9. **In re Claim 8**, Iwasaki teaches the junction field-effect transistor according to Claim 7, further comprising:

- a gate electrode (13, paragraph 0035) formed on the surface of said second conductivity type doped region (52, paragraph 0038) ,
- an electrode, either a source electrode or a drain electrode (11, paragraph 0035), formed on the surface of said first conductivity type semiconductor layer (2, paragraph 0035) and
- another electrode, either a drain electrode or a source electrode (12, paragraph 0035), formed on another main surface (lower surface) of said semiconductor substrate (1, paragraph 0035).

Claim Rejections - 35 USC § 103

10. **The following is a quotation of 35 U.S.C. 103(a)** which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. **Claims 5 and 6 are rejected under 35 U.S.C. 103(a)** as being unpatentable over Iwasaki in view of Kuwata (US 5,331,410).

12. **In re Claim 5**, Iwasaki teaches the junction field-effect transistor according to Claim 4 as cited above. Iwasaki teaches a first conductivity type (n-type) carrier concentration in the first semiconductor layer (2, paragraph 0035), but fails to teach that the transistor further comprising:

- another buffer formed under said channel region on said second conductivity type semiconductor layer, where
- a first conductivity type carrier concentration in said another buffer layer is lower than the first conductivity type cattier concentration in said first conductivity type semiconductor layer.

Iwasaki teaches (Fig. 4B):

- a buffer layer (3, column 2, lines 67-68) formed under a channel region (4, column 3, lines 4-5) on a second conductivity type (p-type) semiconductor layer (2, column 2, lines 62-63), where
- a first conductivity type carrier concentration (n-type) in said buffer layer (3) is equal to zero since the layer contains no dopants (column 2, lines 67-68).

Iwasaki and Kuwata are analogous arts because they both are directed towards transistors, and one of ordinary skill in the art would have had a reasonable expectation of success to modify Iwasaki in view of Kuwata because they are from the same field of endeavor.

It would have been obvious for one of ordinary art at the time of the invention to modify Iwasaki' device by creating another buffer layer under the channel region and having first conductivity carrier concentration lower than in the first semiconductor layer in order to increase the speed of carrier electrons (Kuwata, column 1, lines 49-53).

The process limitation of Claim 5, such as "forming a second conductivity type semiconductor layer by implanting dopant ions" has been considered, but only as related to the structure that must necessarily result from the recited process: In accordance with "*In re Garnero, 412 F2.d 276, 279, 162 USPQ 221, 223 (CCPA 1979)", only "the structure implied by the process steps should be considered when assessing the patentability of product-by-process claims over the prior art".* The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process.

13. **In re Claim 6**, Iwasaki, as modified by Kuwata, teaches the invention of Claim 5 as cited above. Iwasaki teaches first conductivity type carrier (n-type, paragraph 0035) in the semiconductor layer (2, paragraph 0035), but fails to teach another buffer layer having first type conductivity not more than one tenth of said first conductivity type carrier concentration in said first conductivity type semiconductor layer.
Kuwata teaches a buffer layer (3, column 2, lines 67-68) formed under a channel region (4, column 3, lines 4-5) on a second conductivity type (p-type) semiconductor layer (2, column 2, lines 62-63), where a first conductivity type carrier concentration (n-type) in

said buffer layer (3) is equal to zero since the layer contains no dopants (column 2, lines 67-68).

It would have been obvious for one of ordinary art at the time of the invention to modify Iwasaki' device by creating another buffer layer under the channel region and having first conductivity carrier concentration not more than one tenth of said first conductivity type carrier concentration in said first conductivity type semiconductor layer in order to increase the speed of carrier electrons (Kuwata, column 1, lines 49-53).

14. **In re Claim 9**, Iwasaki teaches (Fig. 5) the junction field-effect transistor according to Claim 7, further comprising:

- a gate electrode (13, paragraph 0035) formed on the surface of said second conductivity type doped region (52, paragraph 0038), and
- a source electrode (11, paragraph 0035) formed on the surface of said first conductivity type semiconductor layer (2, paragraph 0035).

Iwasaki fails to teach a drain electrode formed on the same surface as a source electrode.

Kuwata teaches (Fig. 4B) a drain electrode (9, column 3, line 17) and a source electrode (8, line 17) formed on the same surface (6, column 3, lines 17-18).

It would have been obvious for one of ordinary skill in the art at the time of the invention to use the Iwasaki device structure with a buffer layer for a lateral transistor (per Kuwata) in order to improve parameters of lateral transistors and to increase the field of transistors applications.

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

- Fujikawa et al. (US 2006/0113574, the English version of the WO 2004112150, published in December, 2004) and Harada et al. (US 2002/0190258) teach a junction field effect transistor with a buffer layer and a SiC substrate.
- Kuwata et al. (EP 0555886) teaches a junction filed effect transistor having a buffer layer under the channel.
- Kato et al. (US 2002/0003245) teaches a lateral transistor comprising two buffer layers.

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to GALINA YUSHINA whose telephone number is (571)270-7440. The examiner can normally be reached on Monday through Friday, 7:30 to 5, 5/4.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley, can be reached on (571)272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Lynne A. Gurley/
Supervisory Patent Examiner, Art Unit 2811

/Galina Yushina/

Patent Examiner, Art Unit 2811

07/08/09